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Amendments to the Claims

Please amend Claims 28-30, 37 and 39. Please cancel Claim 38. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-27. Canceled.

28. (Currently Amended) A data encryption system comprising:

a control process which modifies a received packet to include control data which includes a list of identifies processes to be performed on the packet;

a plurality of processors which perform the processes identified by the control data, including an encryption process;

an interconnection including a buffer controller which responds to control data in the packet to determine a processor of the plurality of processors dedicated for processing a process in the list of processes and forwards forward the packet with control data ~~from~~ processor to the determined processor; and

an output from which the processed packet is forwarded without the control data upon completion of the processes in the list of processes.

29. (Currently Amended) The system as claimed in Claim 28 wherein the interconnection comprises a packet buffer ~~including a buffer controller which determines a next processor of the plurality of processors to process the data packet.~~

30. (Currently Amended) The system as claimed in Claim ~~29~~ 28 wherein the buffer controller includes a resource manager which maintains information on resource processor availability.

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31. (Previously Presented) The system as claimed in Claim 28 wherein the control data includes code to be processed in at least one of the processors.
32. (Previously Presented) The system as claimed in Claim 28 wherein the control data further includes an encryption or authentication key.
33. (Previously Presented) The system as claimed in Claim 28 wherein individual processors add result data to the control data.
34. (Previously Presented) The system as claimed in Claim 28 wherein the processors perform IPSec protocol processing.
35. (Previously Presented) The system as claimed in Claim 28 wherein respective processors perform IP header manipulation and encryption.
36. (Previously Presented) The system as claimed in Claim 35 wherein a processor performs authentication processing.
37. (Currently Amended) A method of encrypting or decrypting data packets comprising:
 - modifying a received packet to include control data which ~~identifies~~ includes a list of processes to be performed on the packet;
 - forwarding the packet from processor to processor through an interconnection including a buffer controller which responds to control data in the packets to determine a processor of the plurality of processors dedicated for processing a process in the list of processes; and
 - in successive processors, performing the processes identified by the control data, including an encryption or decryption process.
38. Canceled.

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39. (Previously Presented) The method as claimed in Claim ~~38~~ 37 wherein the interconnection comprises a packet buffer ~~including a buffer controller which determines a next processor of the plurality of processors to process the data packet.~~
40. (Previously Presented) The method as claimed in Claim 37 wherein the buffer controller includes a resource manager which maintains information on resource processor availability.
41. (Previously Presented) The method as claimed in Claim 37 wherein the control data includes code to be processed in at least one of the processors.
42. (Previously Presented) The method as claimed in Claim 37 wherein the control data further includes an encryption or authentication key.
43. (Previously Presented) The method as claimed in Claim 37 wherein individual processors add result data to the control data.
44. (Currently Amended) The method as claimed in Claim 37 wherein the processors perform IPSEC protocol processing.
45. (Previously Presented) The method as claimed in Claim 37 wherein respective processors perform IP header manipulation and encryption.
46. (Previously Presented) The method as claimed in Claim 45 wherein a processor performs authentication processing.
47. (New) The data encryption system of claim 28 wherein the control process is executed by a master processor.